M.Tech

(VLSI)

V25 Programme Course Structure & Syllabus

V25 Programme Structure M. Tech (VLSI)

I – Semester

S. No.	Course Code	Subject Name	Subject Code	L	T	P	C
1	PC	Digital CMOS Circuit Design	V252115731	3	1	0	4
2	PC	Analog CMOS Circuit Design	V252115732	3	1	0	4
3	PC	MoS Device Physics	V252115733	3	1	0	4
4	PE-I	VLSI Technology	V2521157D1	3	0	0	3
		Nano Scale Devices	V2521157D2				
		MOS Devices Modeling and Characterization	V2521157D3				
		Digital System Design through HDL	V2521157D4				
5	PE-II	VLSI Architectures	V2521157E1	3	0	0	3
		Power Management IC Design	V2521157E2				
		Low Power Design Techniques	V2521157E3				
		CAD for VLSI	V2521157E4				
6	PC	Digital CMOS Circuit Design Lab	V252115761	0	1	2	2
7	PC	Analog CMOS Circuit Design Lab	V252115762	0	1	2	2
8	Seminar	Seminar-I	V25211CCN1	0	0	2	1
		TOTAL		**15**	**5**	**6**	**23**

CONTROLLER OF EXAMINATIONS **PRINCIPAL**

V25 Programme Structure M.Tech (VLSI)

II – Semester

Sl. No.	Course Code	Subject Name	Subject Code	L	T	P	C
1	PC	CMOS Mixed Signal Circuit Design	V252125731	3	1	0	4
2	PC	Physical Design Verification	V252125732	3	1	0	4
3	PC	VLSI Testing & Testability	V252125733	3	1	0	4
4	PE-III	VLSI signal processing	V2521257F1	3	0	0	3
		MEMS&NEMS	V2521257F2				
		SoC design	V2521257F3				
		Fundamentals of Semiconductor Package Manufacturing and Test	V2521257F4				
5	PE-IV	Advanced VLSI Interconnects	V2521257G1	3	0	0	3
		Quantum Computing	V2521257G2				
		RF IC Design	V2521257G3				
		NANO ELECTRONICS	V2521257G4				
6	PC	CMOS Mixed Signal Circuit Design Lab	V252125761	0	1	2	2
7	PC	Physical Design Verification Lab	V252125762	0	1	2	2
8		Seminar – II	V25212CCN1	0	0	2	1
		TOTAL		**15**	**5**	**6**	**23**

CONTROLLER OF EXAMINATIONS **PRINCIPAL**

V25 Programme Structure M. Tech (VLSI)

III SEMESTER

Sl. No.	Course Code	Subject Name	Subject Code	L	T	P	C
1	PC	Research Methodology and IPR	V25221CC31	3	0	0	3
2	Internship	Summer Internship/ Industrial Training	V25221CC81	-	-	-	3
3	Value Addition Course	Comprehensive Viva	V25221CCK1	-	-	-	2
4	Project Work	Dissertation Part – A	V25221CCA1	-	-	20	10
		TOTAL		**3**	**-**	**20**	**18**

IV SEMESTER

Sl. No.	Course Code	Subject Name	Subject Code	L	T	P	C
1		Dissertation Part – B	V25222CCA1	-	-	32	16
		TOTAL		**-**	**-**	**32**	**16**

CONTROLLER OF EXAMINATIONS **PRINCIPAL**

I Semester	DIGITAL CMOS CIRCUIT DESIGN (V252115731)	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Analyze MOSFET behavior and CMOS inverter characteristics under static and dynamic conditions.	K4
CO2	Design various combinational and sequential logic blocks using CMOS technology.	K5
CO3	Optimize data path elements such as adders, multipliers, and barrel shifters	K4
CO4	Design and evaluate memory architectures including SRAM and ROM cells	K5
CO5	Interpret and implement circuit layouts using stick diagrams and layout rules	K3

Mapping of course outcomes with program outcomes

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	H	M	H	H	M	H
CO2	M	M	H	H	M	H
CO3	M	L	M	H	L	H
CO4	M	L	M	M	M	H
CO5	L	H	M	H	M	M

Unit	Syllabus	Contact Hours
Unit I	**MOS Transistor Principles and CMOS Inverter** : MOSFET characteristics under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter – Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay Parameters, Stick Diagram and Layout Diagrams.	12
Unit II	**Combinational Logic Circuits** : Static CMOS Design, Different Styles of Logic Circuits, Logical Effort of Complex Gates, Static and Dynamic Properties of Complex Gates, Interconnect Delay, Dynamic Logic Gates.	12
Unit III	S **Sequential Logic Circuits** : Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non-Bistable Sequential Circuits.	12
Unit IV	**Arithmetic Building Blocks** : Data Path Circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs.	12
Unit V	**Memory Architectures** : Memory Architectures and Memory Control Circuits: Read-Only Memories, ROM Cells, Read-Write Memories	12

	(RAM), Dynamic Memory Design, 6-Transistor SRAM Cell, Sense Amplifiers.	
	Total	60

TEXT BOOKS:

1. JanRabaey, Anantha Chandrakasan, B Nikolic,"Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2. N.Weste,K.Eshraghian,"PrinciplesofCMOSVLSIDesign",AddisionWesley,2nd Edition, 1993

REFERENCE BOOKS:

1. MJ Smith,"ApplicationSpecificIntegratedCircuits",AddissonWesley,1997
2. Sung-MoKang &Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill,1998

I Semester	ANALOG CMOS CIRCUIT DESIGN (V252115732)	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Design basic building blocks of CMOS Analog ICs.	
CO2	Carry out the design of single and two stage operational amplifiers and voltage references	
CO3	Determine the device dimensions of each MOSFETs involved	
CO4	Design various amplifiers like differential, current and operational amplifiers	

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	H	M	H
CO2	M	M	H	H	M	H
CO3	M	L	M	M	L	M
CO4	M	L	H	H	M	H

Unit	Syllabus	Contact Hours
Unit I	MOS Devices and Modeling: The MOS Transistor, Passive Components - Capacitor & Resistor, Integrated Circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.	12
Unit II	Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors - Current Mirror with Beta Helper, Degeneration, Cascode Current Mirror and Wilson Current Mirror, Current and Voltage References, Bandgap Reference.	12
Unit III	Single Stage Amplifier: Common Source Stage with Resistive Load, Diode Connected Load, Triode Load, CS Stage with Source Degeneration, Source Follower, CG Stage, Gain Boosting Techniques, Cascode, Folded Cascode, Choice of Device Models.	12
Unit IV	CMOS Amplifiers and Noise: Inverters, Differential Amplifiers, Cascode Amplifiers. Noise - Statistical Characteristics, Types, Noise in Single-Stage Amplifiers, Noise in Differential Pairs, Noise Bandwidth.	12
Unit V	CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of Op Amps.	12
	Total	60

TEXT BOOKS:

1. CMOS Analog Circuit Design -Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R.G. Meyer, Wiley India, Fifth Edition, 2010.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

I Semester	MOS DEVICES PHYSICS (V252115733)	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Understand the electrostatics and energy band behavior of MOS structures	K2
CO2	Analyze and model MOSFETs using classical and advanced physical principles	K4
CO3	Evaluate SOI-based MOSFET devices and their operational characteristics	K4
CO4	Apply quantum and ballistic transport concepts to nanoscale transistor design	K3
CO5	Explore and assess modern MOSFET structures including FinFETs and strained-Si devices.	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	H	M	M	M	H	M
CO2	H	M	H	M	H	H
CO3	M	L	H	M	H	M
CO4	H	M	H	M	H	H
CO5	M	M	H	M	H	M

Unit	Syllabus	Contact Hours
Unit I	MOS Capacitor: Energy Band Diagram of Metal-Oxide-Semiconductor Contacts, Modes of Operation – Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV Characteristics of MOS, LFCV and HFCV, Non-Idealities in MOS – Oxide Fixed Charges, Interfacial Charges, Midgap Gate Electrode, Poly-Silicon Contact, Electrostatics of Non-Uniform Substrate Doping, Ultrathin Gate-Oxide and Inversion Layer Quantization, Quantum Capacitance, MOS Parameter Extraction.	12
Unit II	Physics of MOSFET: Drift-Diffusion Approach for I–V Characteristics, Gradual Channel Approximation, Sub-threshold Current and Slope, Body Effect, Pao & Sah Model, Detailed 2D Effects in MOSFET, High Field and Doping Dependent Mobility Models, High Field Effects and MOSFET Reliability Issues (SILC, TDDB, and NBTI), Leakage Mechanisms in Thin Gate Oxide, High-K Metal Gate MOSFET Devices and Technology Issues, Intrinsic MOSFET Capacitances and	12

	Resistances, Meyer Model.	
Unit III	SOI MOSFET: FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, VT Definitions, Back Gate Coupling and Body Effect Parameter, I–V Characteristics of FDSOI-FET, FDSOI Sub-threshold Slope, Floating Body Effect, Single Transistor Latch, ZRAM Device, Bulk and SOI FET – Discussions Referring to the ITRS.	12
Unit IV	Nanoscale Transistors: Diffusive, Quasi-Ballistic, and Ballistic Transports, Ballistic Planar and Nanowire FET Modeling – Semi-Classical and Quantum Treatments.	12
Unit V	Advanced MOSFETs: Strain Engineered Channel Materials, Mobility in Strained Materials, Electrostatics of Double Gate and FinFET Devices.	12
	Total	60

TEXT BOOKS:

1. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, Wiley.
2. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press.
3. M. Lundstrom and J. Guo, *Nanoscale Transistors: Device Physics, Modeling& Simulation*, Springer.

REFERENCE BOOKS:

1. Y. Tsividis, *Operation and Modeling of the MOS Transistor*, Oxford University Press.
2. J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, Springer.
3. Selected research papers in relevant and emerging areas.

I Semester	VLSI TECHNOLOGY (V2521157D1)	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)
CO1	To understand the semiconductor materials, devices and technology historical evaluation	K2
CO2	To analyze the oxidization process and quality measures in the fabrication.	K4
CO3	To explain lithography importance in the semiconductor industry and the various Techniques	K2
CO4	To apply other process steps like etching, implantation and metallization and their applications	K3
CO5	To understand the concepts of electrical testing and packaging of ICs	K2

Mapping of course outcomes with program outcomes

CO\PO	PO1	PO2	PO3	PO4	PO5	
CO1	M	M	H	M	H	
CO2	M	L	M	L	H	
CO3	M	M	H	L	H	
CO4	M	M	H	M	H	
CO5	L	H	M	L	H	

Unit	Syllabus	Contact Hours
Unit I	Introduction: Semiconductor materials, semiconductor devices, semiconductor process technology, basic fabrication steps. Crystal Growth: Silicon crystal growth from melt, silicon float-zone process, GaAs crystal growth techniques, material characterization.	12
Unit II	Silicon Oxidation: Thermal oxidation, impurity redistribution during oxidation, masking of silicon dioxide, oxide quality. Photolithography: Optical lithography, E-beam lithography.	12
Unit III	Etching: Wet chemical etching, dry etching. Diffusion: Basic diffusion process, extrinsic diffusion, lateral diffusion.	12
Unit IV	Ion Implantation: Range of implanted ions, implant damage and annealing. Film Deposition: Epitaxial growth techniques, structures and defects in epitaxial layers, dielectric deposition.	12
Unit V	Process Integration: Passive components, bipolar technology, MESFET technology, MEMS technology. IC Manufacturing: Electrical testing, packaging.	12
	Total	60

Text Books:

1. 1. Gary S May & Simon M Sze, Fundamentals of Semiconductor Fabrication, Wiley Student edition,2012

References:

1. S. K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc, 2010.
2. S. M. Sze, VLSI Technology, 2/e, McGraw Hill, 2011.
3. Stephen Cambell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 2013.

I Semester	VLSI ARCHITECTURES (V2521157E1)	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Design RISC architecture and control units for a given instruction set.	K5
CO2	Improve the performance of RISC processors by applying pipelining techniques	K4
CO3	Translate DSP algorithms into efficient hardware architectures and design associated building blocks	K3
CO4	Analyze the impact of retiming, unfolding, and folding on the performance of DSP architectures	K4

Mapping of course outcomes with program outcomes

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	M	H	H	H	M
CO2	M	M	H	H	H	M
CO3	H	M	H	H	H	H
CO4	M	M	H	M	H	M

Unit	Syllabus	Contact Hours
Unit I	Instruction Set Architectures and CPU Performance: Overview of Instruction Set Architectures – CISC, RISC, and DSP Processors, CPU Performance and Its Factors, Evaluating Performance Metrics.	12
Unit II	Design of RISC Processor: Designing the Datapath and Control Unit for a RISC Processor, Multicycle Implementation of RISC Architecture.	12
Unit III	Enhancing Performance with Pipelining: Overview of Pipelining, Pipelined Datapath, Pipelined Control Unit, Pipeline Hazards – Data, Control, and Structural Hazards, Techniques for Hazard-Free Pipelined RISC Implementation.	12
Unit IV	Multiprocessors and DSP Algorithm Representation: Introduction to Multiprocessors, Multiprocessors Connected by a Single Bus and Network, Network Topologies, Evolution vs. Revolution in Computer Architecture, DSP Algorithm Representation – Data Flow Graphs, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound.	12
Unit V	Pipelining, Parallel Processing, and VLSI Performance Techniques: Introduction to Pipelining and Parallel Processing, FIR Filter Pipelining, Parallel Processing Techniques, Pipelining and Parallel Processing for Low Power, VLSI Architecture Optimization Techniques – Retiming, Unfolding, and Folding.	12
	Total	60

TEXT BOOKS:

1. D.A,Patterson And J.L.Hennessy, Computer Organization and Design: Hardware/ Software Interface, Elsevier, 2011, 4th Edition
2. Keshab Parhi, VLSI digital signal processing systems design and Implementations, Wiley 1999
3. NPTEL Courses (https://nptel.ac.in/courses/108105157)

I Semester	ANALOG CMOS CIRCUIT DESIGN LAB (V252115762)	L	T	P	C
		0	1	2	2

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools	K3
CO2	Grasp the significance of various cmos analog circuits in full-custom IC Design flow	K4
CO3	Have the ability to explain the Physical Verification in Layout Design	K3
CO4	Fully Appreciate the design and analyze of analog and mixed signal simulation	K4
CO5	Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation	K5

List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. simple current mirror
6. cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:

Software:

Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator/ Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

I Semester	DIGITAL CMOS CIRCUIT DESIGN LAB (V252115761)	L	T	P	C
		0	1	2	2

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools	K3
CO2	Grasp the significance of various design logic Circuits in full-custom IC Design.	K4
CO3	Have the ability to explain the Physical Verification in Layout Extraction	K3
CO4	Fully Appreciate the design and analyze of CMOS Digital Circuits	K4
CO5	Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation	K5

List of Experiments:

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Industry Standard Software (Mentor Graphics Tool/Cadence/ Synopsys/Equivalent)

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

II Semester	CMOS MIXED SIGNAL CIRCUIT DESIGN (V252125731)	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Understand the necessity of mixed signal systems	K2
CO2	Analyze Op-Amp to meet the mixed signal specifications	K4
CO3	Design CMOS comparators to meet the high-speed requirements of digital circuitry	K5
CO4	Develop efficient data converter circuits for mixed signal systems	K4

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	M	H
CO2	L	L	M	H	M	H
CO3	M	M	M	H	H	H
CO4	M	L	M	H	H	H

Unit	Syllabus	Contact Hours
UNIT - I	Two-Stage OP-AMP Design :Parasitic Effects on Design of Two-Stage OP-AMP, Wide-Swing Cascode Current Mirrors, Design of Rugged Biasing Circuit with Temperature-Independent Compensation, Challenges in Mixed-Signal Circuit Design. Switched Capacitor Circuits : Constituents: Op-Amp, Capacitors, Switches, Non-overlapping Clocks; Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Design of Filters Based on Switched Capacitor Circuits.	12
UNIT - I	Sample-and-Hold Circuit: Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Charge-Injection Errors, Making Charge-Injection Signal Independent, Minimizing Errors Due to Charge-Injection, Effect of Offset and Application of Switched Capacitor Circuits to Minimize Offset Errors, Parasitic Effects.	12
UNIT - III	Comparators: Ideal Comparator, Practical Model of Comparator, Resolving Capability, Propagation Delay, Small Signal Analysis, Conditions for Slewing, Evaluation of Propagation Delay for Single Pole and Two Pole Comparators, Design of Linear Response Comparators, Slew-Rate Limited Comparators, Comparators with Positive Feedback, Analysis of Latched Comparators, Architecture of	12

	High-Speed Comparators, Self-Biased Comparators, Push Pull Comparators.	
UNIT - IV	Data Converters : Classification, Ideal D/A Converter, Ideal A/D Converter, Quantization Noise: Deterministic and Stochastic Approach, Signed Codes, Performance Limitations: Resolution, Offset and Gain Error, Accuracy and Linearity, Integrating Converters, Design of Successive-Approximation Converters, DAC-Based and Charge-Redistribution SAR, Interleaved, Pipelined, Flash, Principles of Sigma-Delta ADC, Testing of Data Converters.	12
UNIT - V	PLL and Oscillators : Basic PLL Architecture, VCO, Divider, Phase Detector, Loop Filter, PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model, Limitations, PLL Characterization and Design Example, Jitter and Phase Noise: Period Jitter, Cycle Jitter, Adjacent Period Jitter, Spectral Representations and PDF of Jitter, Ring and LC Oscillators, Phase Noise in Oscillators and PLLs.	12
	Total	60

TEXT BOOKS:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits"McGraw Hill Education, 2017, 2nd Edition.
3. R.JacobBaker,CMOS:Mixed-SignalCircuitDesign,Wiley,2008,2nd Edition.

REFERENCE BOOKS:

1. Roubik Gregorian and Gabor C. Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.
2. Roubik Gregorian, Introduction to CMOS Op-Amps and Comparators, Wiley, 2008.
3. RuiPauloda Silva Martins and Pui-InMak,"Analog and Mixed-Signal Circuits in Nano scale CMOS", Springer, 2024.

Other Suggested Readings:

- NPTELCourses(https://onlinecourses.nptel.ac.in/noc22_ee34/preview)

II Semester	PHYSICAL DESIGN VERIFICATION (V252125732)	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology	K2
CO2	Adapt the design algorithms to meet the critical design parameters.	K3
CO3	Identify layout optimization techniques and map them to the algorithms	K3
CO4	Develop proto-type EDA tool and test its efficacy	K4

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	H	H	M
CO2	L	M	M	H	M	M
CO3	M	M	M	H	H	L
CO4	H	M	H	H	M	M

Unit	Syllabus	Contact Hours
UNIT I	VLSI Design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication. Design styles: Full Custom, Standard Cell, Gate Arrays, Field Programmable Gate Arrays, Sea of Gates and Comparison, System Packaging Styles, Multi-Chip Modules. Design Rules, Layout of Basic Devices, Fabrication Process and Its Impact on Physical Design, Interconnect Delay, Noise and Crosstalk, Yield and Fabrication Cost.	12
UNIT II	Factors, Complexity Issues and NP-hard Problems. Basic Algorithms (Graph and Computational Geometry): Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Matching Algorithms, Min-Cut and Max-Cut Algorithms, Steiner Tree Algorithms.	12
UNIT III	Basic Data Structures: Atomic Operations for Layout Editors, Linked List of Blocks, Bin Based Methods, Neighbour Pointers, Corner Stitching, Multi-Layer Operations.	12
UNIT IV	Graph Algorithms for Physical Design: Classes of Graphs, Graphs Related to a Set of Lines, Graphs Related to a Set of Rectangles, Graph Problems in Physical Design, Maximum Clique and Minimum Coloring, Maximum k-Independent Set Algorithm, Algorithms for Circle Graphs.	12

UNIT V	Partitioning Algorithms: Design Style Specific Partitioning Problems, Group Migrated Algorithms, Simulated Annealing and Evolution. Floor Planning and Pin Assignment, Routing and Placement Algorithms.	12
	Total	60

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

II Semester	VLSI TESTING & TESTABILITY (V252125733)	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Identify the significance of testable design	K3
CO2	Understand the concept of yield and identify the parameters influencing the same	K2
CO3	Specify fabrication defects, errors, and faults	K3
CO4	Implement combinational and sequential circuit test generation algorithms	K4
CO5	Identify techniques to improve fault coverage	K5

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	L	L	M	H	M	L
CO2	M	M	M	H	H	M
CO3	M	L	M	H	H	M
CO4	M	M	M	H	M	H
CO5	M	L	M	H	H	M

Unit	Syllabus	Contact Hours
UNIT I	Role of Testing in VLSI Design Flow, Testing at Different Levels of Abstraction, Fault, Error, Defect, Diagnosis, Yield. Types of Testing, Rule of Ten, Defects in VLSI Chip. Modelling Basic Concepts, Functional Modelling at Logic Level and Register Level, Structure Models, Logic Simulation, Delay Models. Various Types of Faults, Fault Equivalence and Fault Dominance in Combinational and Sequential Circuits.	12
UNIT II	Fault Simulation Applications, General Fault Simulation Algorithms: Serial and Parallel, Deductive Fault Simulation Algorithms.	12
UNIT III	Combinational Circuit Test Generation, Structural Vs Functional Test, ATPG, Path Sensitization Methods. Difference Between Combinational and Sequential Circuit Testing, Five and Eight Valued Algebra, Scan Chain-Based Testing Method.	12
UNIT IV	D-Algorithm Procedure, Problems. PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN Algorithm. Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-Hoc Design, Generic Scan-Based Design.	12

UNIT V	Classical Scan-Based Design, System Level DFT Approaches. Test Pattern Generation for BIST, Circular BIST, BIST Architectures. Testable Memory Design: Test Algorithms, Test Generation for Embedded RAMs.	12
	Total	60

TEXT BOOKS:

1. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. M. Bushnell and V. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.

REFERENCE BOOKS:

1. Stroud,"A Designer's Guide to Built-in Self-Test", Kluwer AcademicPublishers,2002
2. V.Agrawal and S.C.Seth, Test Generation for VLSI Chips, Computer Society Press. 1989

Other Suggested Readings:

1. NPTELCourses(https://archive.nptel.ac.in/courses/117/105/117105137/)

II Semester	FUNDAMENTALS OF SEMICONDUCTOR PACKAGE MANUFACTURING AND TEST (V2521257F4)	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Understand the evolution of semiconductor packaging technologies and explain the various backend assembly processes involved in IC packaging.	K2
CO2	Analyze the selection and role of substrate materials, interconnect technologies, and encapsulation methods, along with reliability challenges like delamination and thermal cycling.	K4
CO3	Demonstrate knowledge of electrical and mechanical test techniques at both wafer and package levels, including DC/AC testing, BIST, JTAG, and mechanical integrity tests.	K5
CO4	Apply reliability concepts, failure analysis techniques, and quality control methodologies to assess and improve package manufacturing outcomes.	K4
CO5	Evaluate advanced and emerging semiconductor packaging trends such as 3D stacking, TSVs, RF/MEMS packaging, and environmentally sustainable practices through industry case studies.	K5

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	H	H	L
CO2	M	M	M	H	H	M
CO3	M	M	M	H	H	M
CO4	H	M	M	H	H	M
CO5	H	M	H	M	H	M

Unit	Syllabus	Contact Hours
UNIT I	Overview of Semiconductor Packaging and Assembly: Semiconductor Packaging Evolution and Types (e.g., BGA, LGA, Flip Chip). Backend Assembly Processes: Wafer Dicing, Die Attach, Wire Bonding, Flip-Chip Bonding, Encapsulation/Molding, Marking.	12
UNIT	Package Substrate and Interconnect Technology: Substrate Materials	12

II	and Package Interconnections, Role of Glues, Underfill, and Encapsulants. Introduction to Package Interconnect Reliability (Delamination, Thermal Cycling).	
UNIT III	Electrical and Mechanical Testing of Packages: Wafer-Level Test, Package-Level Test, Final IC Test. Test Equipment Overview: DC, AC, Functional Tests. Built-In Self-Test (BIST), JTAG Boundary Scan, and Burn-In Testing. Mechanical Tests: Shear, Bend, Pull Strength.	12
UNIT IV	Reliability, Failure Analysis, and Quality Control: Reliability Fundamentals: Bathtub Curve, Failure Mechanisms, Failure Rate Modeling. Process Control Systems for Package Manufacturing Quality. Failure Analysis: Visual Inspection, Decapsulation, X-ray, Electrical Test Correlation.	12
UNIT V	Industry Case Studies & Emerging Packaging Trends: 3D-Stacked Packages, Multi Die Integration, High Density Interposers. Packaging for RF, MEMS, and Sensor Applications. Emerging Materials and Processes: Micro Bump, Through Silicon Vias (TSV), Advanced Substrates. Environmental and Sustainability Considerations in Packaging.	12
	Total	60

Books Recommended

1. Veena Chakravarthi, *A Practical Approach to VLSI System on Chip (SoC) Design – A Comprehensive Guide*, Springer, 2020.
2. S. Pasricha and N. Dutt, *On-Chip Communication Architectures: System on Chip Interconnect*, Morgan Kaufmann–Elsevier Publishers, 2008.
3. Michael Keating, *The Simple Art of SoC Design*, Springer, 2011.
4. Patrick Schaumont, *A Practical Introduction to Hardware/Software Co-design*, Springer, 2009.
5. François Ghenassia, *Transaction-Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems*, Springer, 2010.
6. Wolfgang Grotker, Shuqing Liao, Grant Martin, and Stuart Swan, *System Design with SystemC*, Springer, 2002.

II Semester	QUANTUM COMPUTING (V2521257G2)	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Understand the fundamental principles of quantum computation and the concept of qubits.	K2
CO2	Analyze multi-qubit systems and quantum communication protocols.	K4
CO3	Analyze multi-qubit systems and quantum communication protocols.	K4
CO4	Design and implement basic quantum algorithms and quantum circuits.	K5
CO5		

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	M	M
CO2	M	L	M	M	M	M
CO3	M	L	M	M	M	M
CO4	M	L	M	M	M	M

Unit	Syllabus	Contact Hours
UNIT I	Review of Quantum Mechanics and Motivation for Quantum Computation. Qubit: The Qubit State - Matrix and Bloch Sphere Representation - Computational Basis - Unitary Evolution.	12
UNIT II	Multi-Qubit States: No-Cloning Theorem, Superdense Coding, Pure States to Bell States, Bell Inequalities. Protocols with Multi-Qubits: Swapping, Teleportation. Gates: CNOT, Toffoli Gate, NAND, FANOUT, Walsh-Hadamard.	12
UNIT III	Measurement: Projective Operators - General, Projective and POVM Measurement. Ensemble: Density Operators - Pure and Mixed Ensemble - Time Evolution - Post Measurement Density Operator. Composite Systems: Partial Trace, Reduced Density Operator, Schmidt Decomposition, Purification, Bipartite Entanglement.	12
UNIT IV	Quantum Computing: Classical Computing Using Qubits, Quantum Parallelism, Deutsch's Algorithm, Deutsch-Jozsa Algorithm.	12
UNIT V	Quantum Circuits: Basic Gates, ABC Decomposition, Gray Codes, Universal Gates, Principle of Deferred and Implicit Measurements. Quantum Fourier Transform and Applications: Phase Estimation, Order	12

	Finding, Factoring, Discrete Logarithm, Hidden Subgroup Problems. Role of Prime Factoring in Classical Cryptography. Search Algorithms, Quantum Error Correcting Codes, Physical Realization of Qubits.	
	Total	60

Text Books:

1. M.A.Nielsen and I.L.Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 2010, 10th Anniversary Edition
2. Chris Bernhardt, Quantum Computing for Everyone, The MITPress,2019.
3. RayLaPierre, Introduction to Quantum Computing,Springer,2021.

Reference Books:

1. Quantum Theory: Concepts and Methods, AsherPeres, Kluwer Academic Publishers,1993.
2. Venkateswaran Kasirajan, Fundamentals of Quantum Computing: Theory and Practice, Springer, 2021.

Other Suggested Readings:

1. NPTELCourses(https://nptel.ac.in/courses/106106232

II Semester	CMOS MIXED SIGNAL CIRCUIT DESIGN LAB (V252125761)	L	T	P	C
		0	1	2	2

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Implement discrete-time signal processing circuits tailored for mixed-signal system requirements	K4
CO2	Apply layout methodologies and design techniques specific to mixed-signal integrated circuits to ensure signal integrity and performance	K3
CO3	Design operational amplifiers optimized for operation in mixed-signal environments with appropriate gain, bandwidth, and stability	K5
CO4	Design high-speed comparators with enhanced resolution and low latency for time-critical mixed-signal application	K5
CO5	Develop data converters and RF circuits considering performance trade-offs in mixed-signal design scenarios.	K4

Mapping of course outcomes with program outcomes

Cycle	Syllabus	
Cycle 1	1) Fully compensated op-amp with resistor and Miller compensation 2) Comparator design: a. Linear Response b. Slew-rate limited	
Cycle 2	3) Switched capacitor circuits: i. Parasitic sensitive integrator ii. Parasitic insensitive integrator iii. Delay free integrators iv. Low Pass filter 4) Data converters (ADC, DAC for given specifications) 5) Layouts and parasitic extraction	

Text Books:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Roubik Gregorian and Gabor C.Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.

Reference Books:

1. Roubik Gregorian, Introduction to CMOS Op-Amp and Comparators, Wiley,1999.
2. Alan Hastings, Theart of Analog Layout, Wiley, 2005

Other Suggested Readings:

1. NPTELCourses(https://onlinecourses.nptel.ac.in/noc23_ee142/preview)

II Semester	PHYSICAL DESIGN VERIFICATION LAB (V252125762)	L	T	P	C
		0	1	2	2

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)
CO1	Implement and analyze graph-based algorithms used in physical design automation, including depth-first search, breadth-first search, spanning trees, and shortest path algorithms	K4
CO2	Apply computational geometry techniques such as line sweep and extended line sweep methods in geometric problem-solving relevant to VLSI layout	K3
CO3	Design and evaluate partitioning algorithms including Kernighan–Lin, Fiduccia–Mattheyses, and Goldberg–Burstein algorithms, as well as simulated annealing and evolution-based approaches	K5
CO4	Implement floorplanning techniques using constraint-based, integer programming, hierarchical tree, rectangular dualization, and simulated evolution strategies	K4
CO5	Develop and compare routing algorithms for two-terminal and multi-terminal nets, including maze routing and Steiner tree-based algorithms like SMST and Z-RST	K4

Mapping of course outcomes with program outcomes

Cycle	Syllabus	
Cycle 1	1) Graph algorithms: a) Graph search algorithms: i. Depth first search ii. Breadth first search b) Spanning tree algorithm: i. Kruskal's algorithm c) Shortest path algorithm: i. Dijkstra algorithm ii. Floyd-Warshall algorithm d) Steiner tree algorithm	
Cycle 2	2) Partitioning algorithms: a. Kernighan–Lin algorithm b. Fiduccias–Mattheyses algorithm c. Simulated annealing and evolution algorithms 3) Floor planning algorithms: i) Constraint based methods ii) Integer programming based methods iii) Rectangular dualization based methods	

	iv) Simulated evolution algorithms 4) Routing algorithms - Two terminal algorithms: a) Maze routing algorithms: i) Lee's algorithm ii) Soukup's algorithm iii) Hadlock algorithm b) Line-Probe algorithm c) Shortest path based algorithm	

Software required: C/C++ Programming Language /Relevant software

Reading:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.